

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 09-153797

(43)Date of publication of application : 10.06.1997

(51)Int.Cl.

H03L 7/093

H04L 7/033

H04N 5/06

(21)Application number : 07-313803

(71)Applicant : MATSUSHITA ELECTRIC IND CO LTD

(22)Date of filing : 01.12.1995

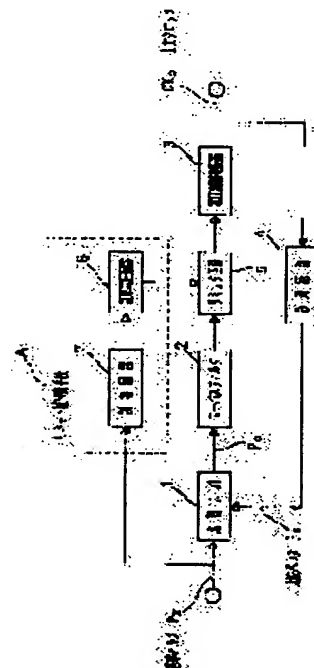
(72)Inventor : OZAWA KENJI

(54) PLL CIRCUIT

(57)Abstract:

PROBLEM TO BE SOLVED: To suppress the malfunction of circuit connected on a rear stage with a phase locked loop (PLL) circuit for the digital signal processing of video signal processing.

SOLUTION: A limiter circuit 5 for limiting the output of low-pass filter (LPF) 2 is interposed between the LPF 2 and a voltage controlled oscillator 3, and a limit value control means A is provided for controlling the limit value of this limiter circuit 5 corresponding to the frequency change of reference pulse PH. Thus, the malfunction of digital processing circuit connected at the back of PLL circuit can be suppressed and the stable time of PLL circuit can be shortened. Further, by switching a limit voltage for each frequency to be switched, the LPF can be easily designed and the stable time of PLL circuit can be optimized as well.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]